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AN IMPROVED WALLEYE TELEVISION CAMERA

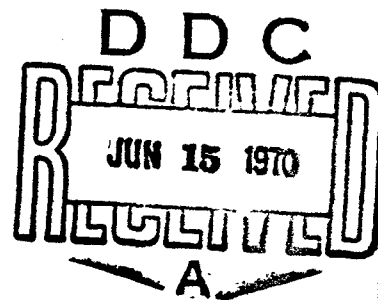
(U)

by

William Woodworth

Aviation Ordnance Department

ABSTRACT. (U) A description of an improved television camera for the Walleye missile with emphasis on the electronic circuitry.



NAVAL WEAPONS CENTER
CHINA LAKE, CALIFORNIA • MAY 1970

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FOREWORD

This report has been prepared primarily for timely presentation of information. Although care has been taken in the preparation of the technical material presented, conclusions drawn are not necessarily final and may be subject to revision.

This work was performed under WepTask A05-510-102/231-1/W11-02.

This report was reviewed for technical accuracy by Marc L. Moulton and Jack A. Crawford.

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INTRODUCTION

(C) This report describes the improved Walleye television (TV) camera that was specifically designed to meet the requirements of the Improved Walleye guidance system. In this system, the volume available for the camera was considerably less than that in the original Walleye. As a result, a shorter vidicon was employed to gain more longitudinal space, and integrated circuit components were used so that most of the electronics occupy a single printed-circuit module.

(C) In addition to reconfiguring the system, the performance was improved, adjustment procedures were simplified, and a practical "electronic zoom" method was developed.

CAMERA DESIGN

(U) The new camera design characteristics are

1. High-resolution, all-magnetic vidicon.
2. Integrated circuit components where there is an obvious advantage in cost, size, and performance.
3. Synchronizing waveform, which is close to standard, with a controlled front and back porch on the horizontal sync and a vertical sync waveform, which is phase-locked to the horizontal. A pedestal level also has been added. (These items make the system compatible with video tape recorders and most types of display devices.)
4. Insulated-gate metal-oxide-semiconductor (MOS) field-effect transistor in the video preamplifier to minimize radio frequency interference (RFI) and improve the video signal-to-noise ratio.
5. Improved video keyed-clamp for stable black-level control, followed with a blacker-than-black clipper to eliminate the white border around the raster and clean up the blanking interval.
6. Video output stage (line driver) with a high-output impedance to reduce the effect of ground potential interference (400-hertz pickup, rat noise, aircraft wiring, and power interference) in aircraft installations.

7. Automatic target system with a fast response time and no level adjustment,

8. Electronic zoom capability by underscanning the vidicon is accomplished instantaneously while the center of the picture remains fixed.

(U) The entire electronic package is simple and compact so that the camera circuitry (except the preamplifier and electrode supplies) can be mounted on a single printed-circuit board.

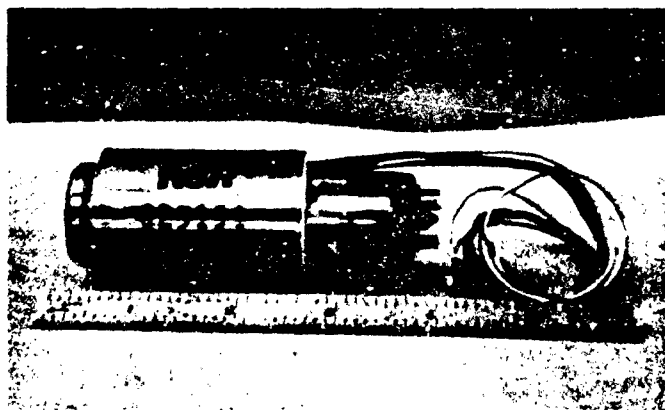
SYSTEM COMPONENTS

(U) In lieu of an overall circuit diagram, the various components of the system are individually described. The main subsections are shown separately and interconnections are indicated in each instance.

VIDICON

(U) The vidicon is an RCA developmental type C23151, all-magnetic unit with the focus and deflection coils permanently bonded to the tube. By this means, the normal alignment and yoke-adjusting procedures are eliminated.

(U) The tube (Fig. 1) has a limiting resolution of approximately 1,200 lines, a response peak of 4,500 to 5,000 angstroms, and an overall length of 4 inches.



(U) FIG. 1. Vidicon Tube.

DEFLECTION CIRCUITS

(U) The deflection circuits for the tube were specially designed for good DC stability and linearity. In addition, they are capable of a 2 to 1 gain change by an external control signal, without any shift of the raster center. The most logical way to accomplish the gain change was to stepwise alter the gain of the deflection amplifiers by changing the value of the series feedback resistors, R_s (Fig. 2 and 3). The deflection amplifiers have no DC input (capacitive-coupling from the ramp generators) so that the change in gain does not cause a DC level shift in the deflection current. Therefore, the picture expands linearly about the raster center as the deflection current is reduced.

(U) The horizontal circuit (Fig. 2) uses discrete components because of the voltage, power, and slew-rate requirements. The ramp generator is a simple R-C charging circuit with a long time constant. The voltage at P_1 is approximately 1 volt, peak-to-peak. Transistors Q_4 , Q_5 , Q_6 , Q_7 , and Q_8 form an operational amplifier with feedback via R_s , R_f , and C_f . Components C_i and R_i correct the yoke-current waveform.

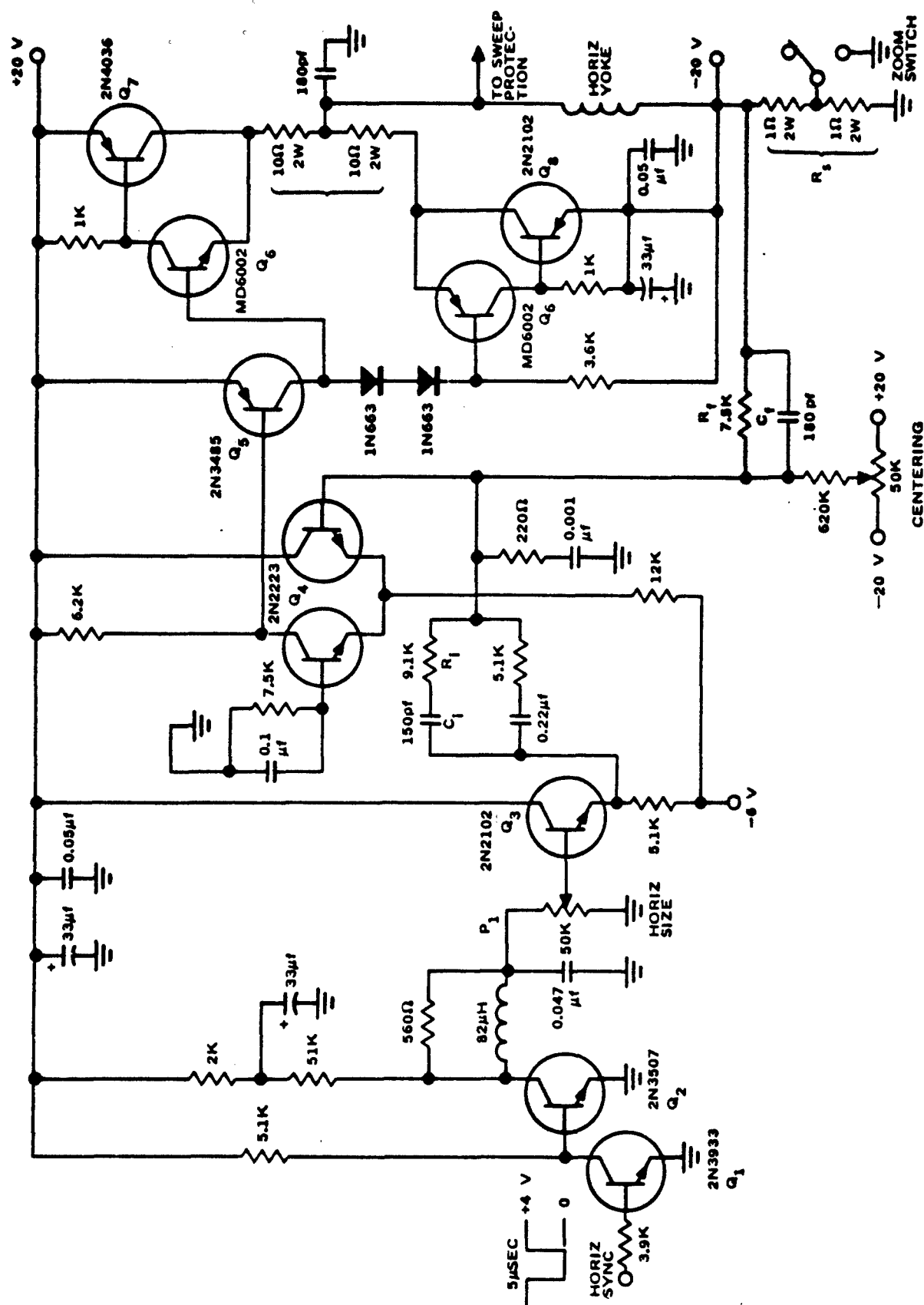
(U) The yoke inductance is approximately 200 microhenries and requires 400 milliamperes, peak-to-peak, for full deflection. The circuit is powered by regulated ± 20 volts. Unregulated voltages can be used, but extreme caution is needed to avoid clipping the flyback pulse and thereby adding power supply ripple into the deflection current.

(U) The vertical deflection circuit (Fig. 3) is similar in function to the horizontal deflection circuit, but integrated circuit components can be used in certain locations. The ramp generator is an analog integrator (IC-1) with about 1-volt, peak-to-peak, output at P_2 . The output amplifier is composed of IC-2, Q_3 , Q_4 , and Q_5 ; feedback is via R_s and R_f . The electronic zoom capabilities are the same as for the horizontal deflection circuit and the yoke characteristics are identical.

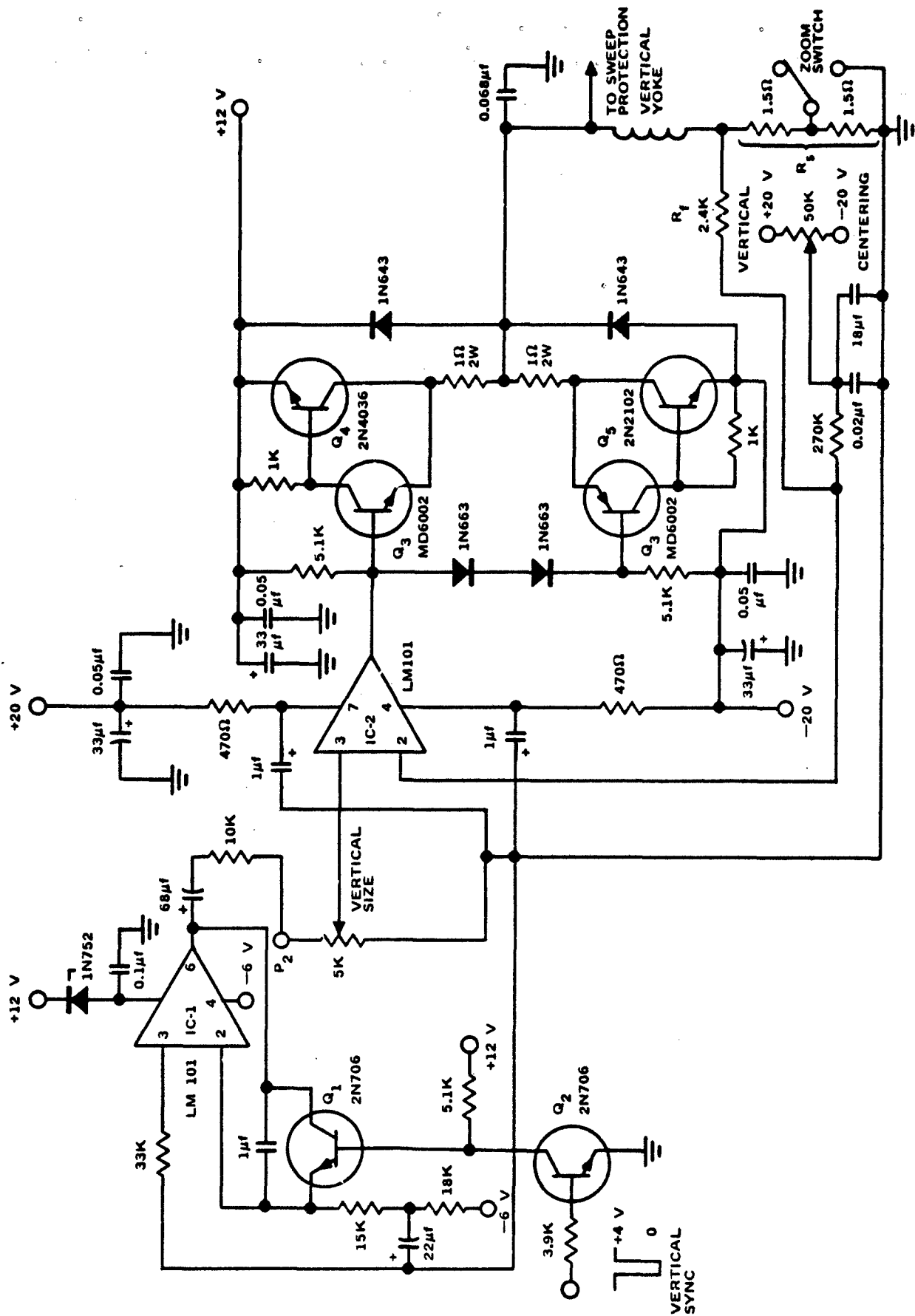
SYNCHRONIZING GENERATOR

(U) The generator is a crystal-controlled digital counter with multiple outputs for sync and clamping. The oscillator is shown in Fig. 4. IC-1 is an amplifier that has positive feedback via X and provides output at 63 kilohertz. The NAND gate, CD 2201, converts to the logic level and IC-2 counts down to 31.5 kilohertz.

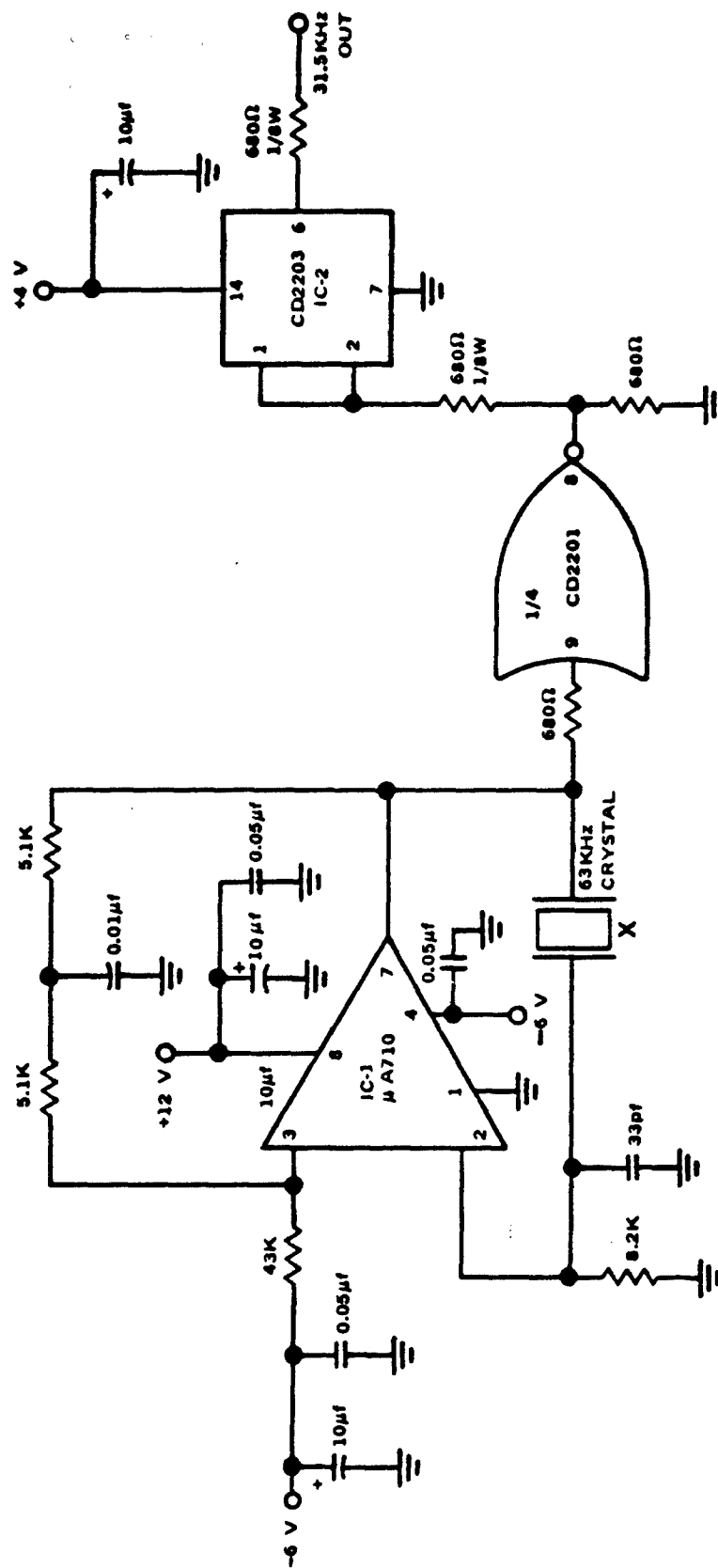
(U) The 31.5-kilohertz signal is fed to the sync generator (Fig. 5). The main part is a ripple-carry counter that divides the input by a factor of 525 to obtain the 60-hertz vertical output. In addition,



(U) FIG. 2. Horizontal Deflection Circuit.

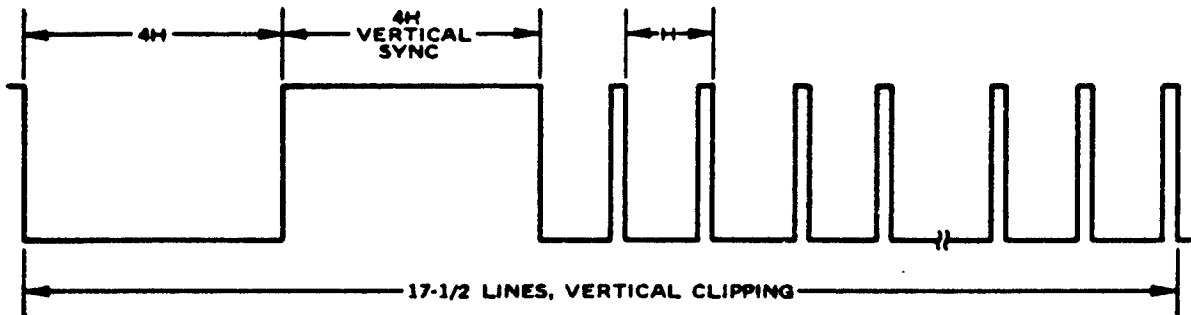


(U) FIG. 3. Vertical Deflection Circuit.



(U) FIG. 4. Oscillator.

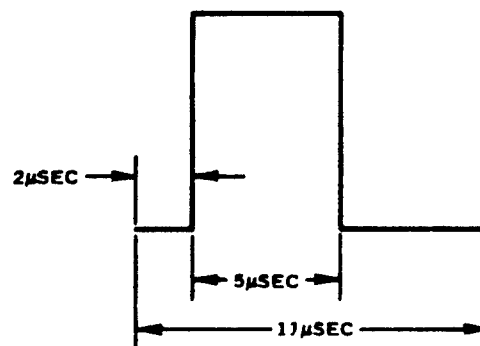
various outputs are decoded to obtain vertical sync and vertical clipping. The horizontal waveforms are not decoded, but generated by one-shot multivibrators, 951-1, -2, and -3. The vertical sync and clipping waveform is shown in Fig. 6.



(U) FIG. 6. Vertical Sync and Clipping Waveform.

(U) In this system, the vertical sync pulse is the retrace drive to the vertical deflection circuit. Vidicon blanking is obtained from an auxiliary circuit (see Fig. 8) triggered from the sync pulse and made slightly longer to avoid retrace edge effects. The empty, four-line period at the beginning of clipping is the vertical rest interval. It allows the integrator in vertical sync-separator systems to become discharged and ready to trigger on the vertical sync pulse. Interlace on the display is preserved by this means. The clipping signal normally would be the blanking signal. In this case, it is applied to the video amplifier and causes all video in the interval to be clipped at the black level. In this sense, it is a blanking signal, but it is not applied to the vidicon.

(U) The horizontal waveform is shown in Fig. 7. The total horizontal clipping interval is 11 microseconds. A front porch of 2 microseconds precedes a 5-microsecond sync pulse. As with the vertical deflection



(U) FIG. 7. Horizontal Sync and Clipping Waveform.

circuit, the sync pulse retraces the horizontal deflection circuit and triggers a slightly longer vidicon blanking pulse. The clipping signal is sent to the video amplifier and clips the video to black during that time.

(U) The remaining components combine horizontal and vertical synchronizing waveforms to form the composite sync, which is used to operate the keyed-clamp, and is also added to the video amplifier output stage to form the composite signal.

VIDICON BLANKING AND SWEEP-FAILURE PROTECTION

(U) The vidicon blanking and sweep-failure protection is provided by the circuit in Fig. 8. Here, IC-1 and IC-2 generate the blanking pulses. Transistors Q₄ and Q₅ combine them while Q₆ amplifies and sends the positive pulses to the vidicon cathode.

(U) The sweep-failure protection senses the voltage at the top of the yokes, rectifies peak-to-peak, and shuts off Q₁ and Q₂. A failure of either voltage causes one of these to turn on. Thus, Q₃ goes off and G₁ is biased to cut off. The potentiometer, T, sets the operating bias voltage.

VIDICON ELECTRODE

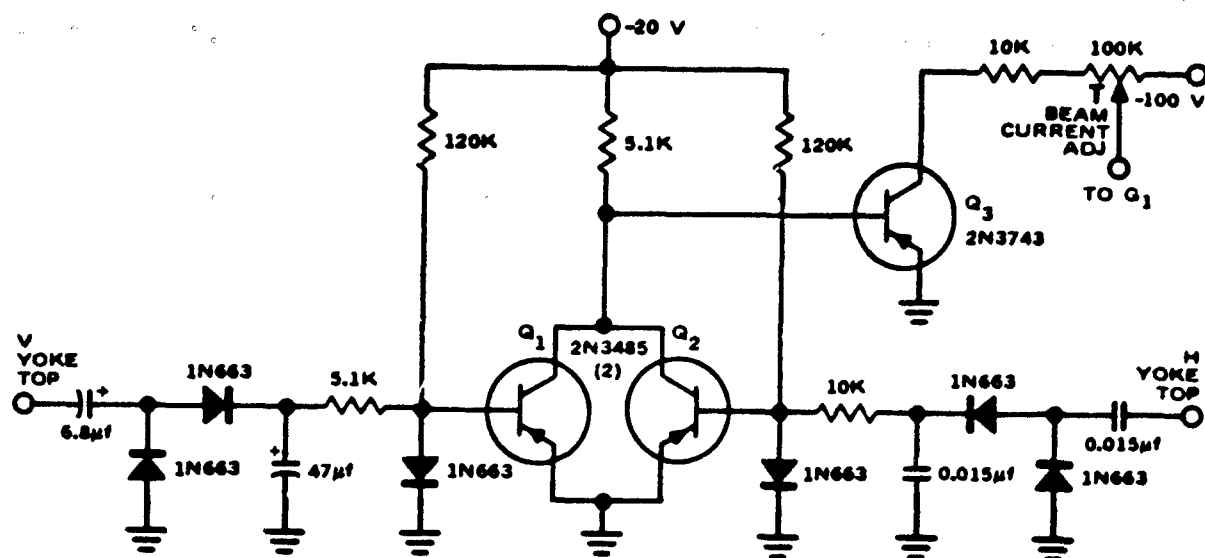
(U) The vidicon electrode high voltages are supplied by a regulated +500-volt source and an emitter-follower amplifier (Fig. 9).

(U) The emitter-follower supplies low-impedance voltage to G₂, and G₃ so that blanking and beam current variations do not affect these electrodes. Otherwise, a low-impedance divider must be used with high-power drain.

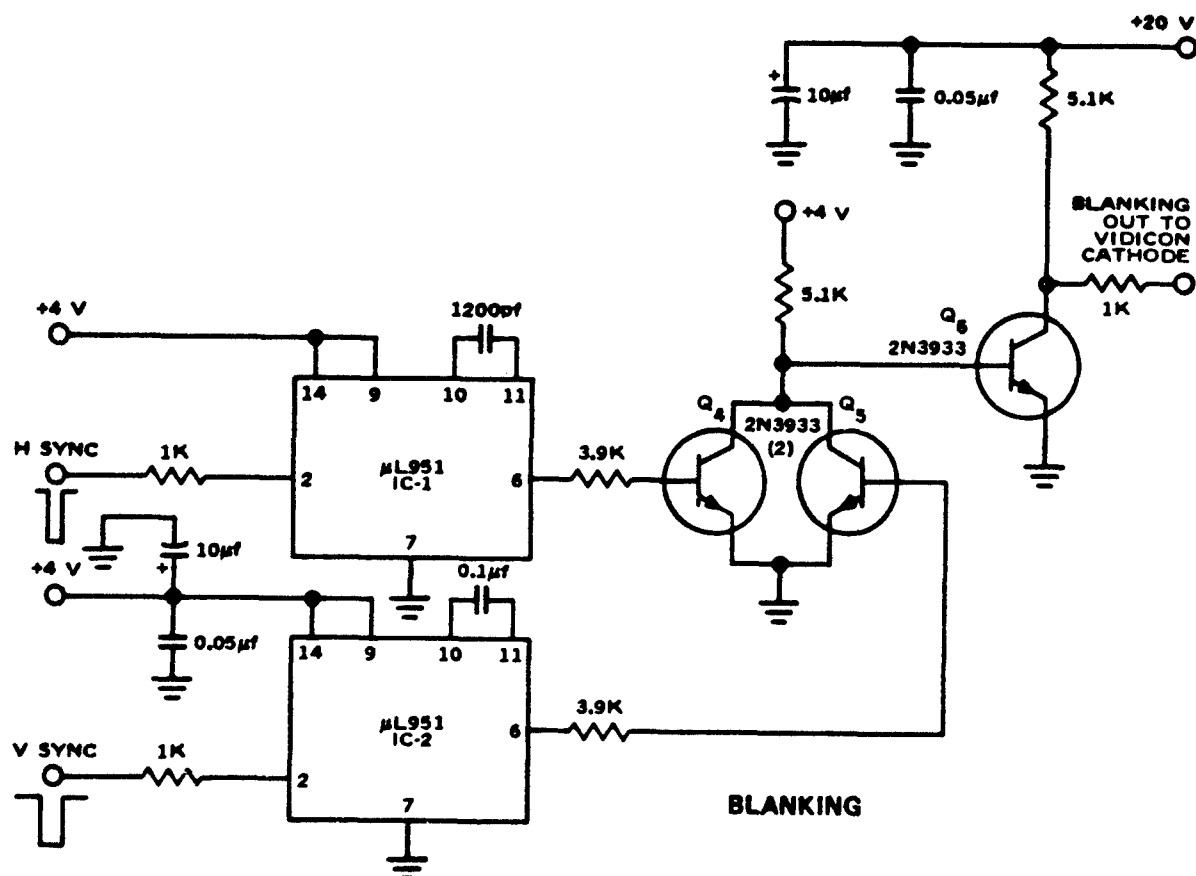
FOCUS CURRENT-REGULATOR

(U) The focus current-regulator is a precision current source of approximately 100 millamperes. It is referenced, in part, to both the high-voltage supply and a fixed supply. Figure 10 gives details of the regulator circuit.

(U) The required focus current varies as the square-root of the high voltage supply. In the interest of practicality, a linear approximation is made by the circuit, wherein a fixed bias supplies one-half the nominal focus current and the rest is made proportional to the high voltage. A simple approximation like this allows the high voltage to vary $\pm 20\%$ without any degradation in focus. The focus regulator must

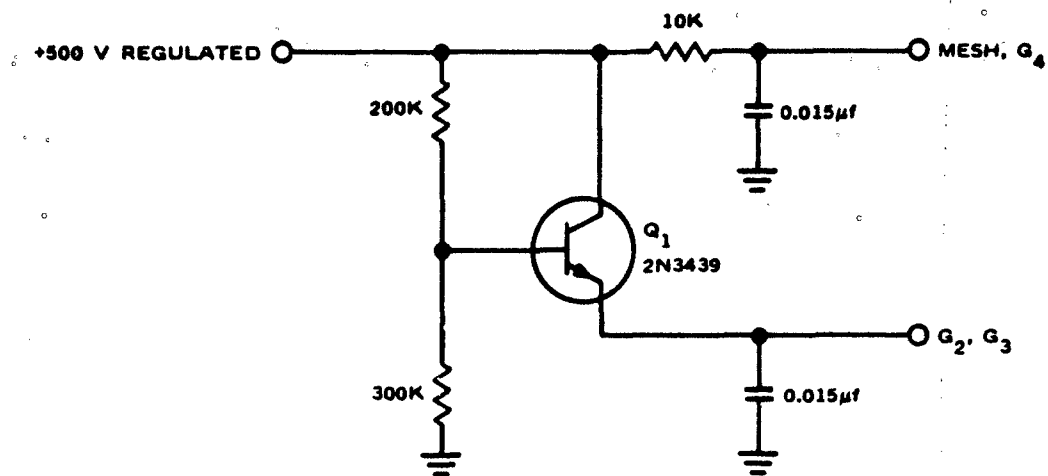


SWEEP PROTECTION



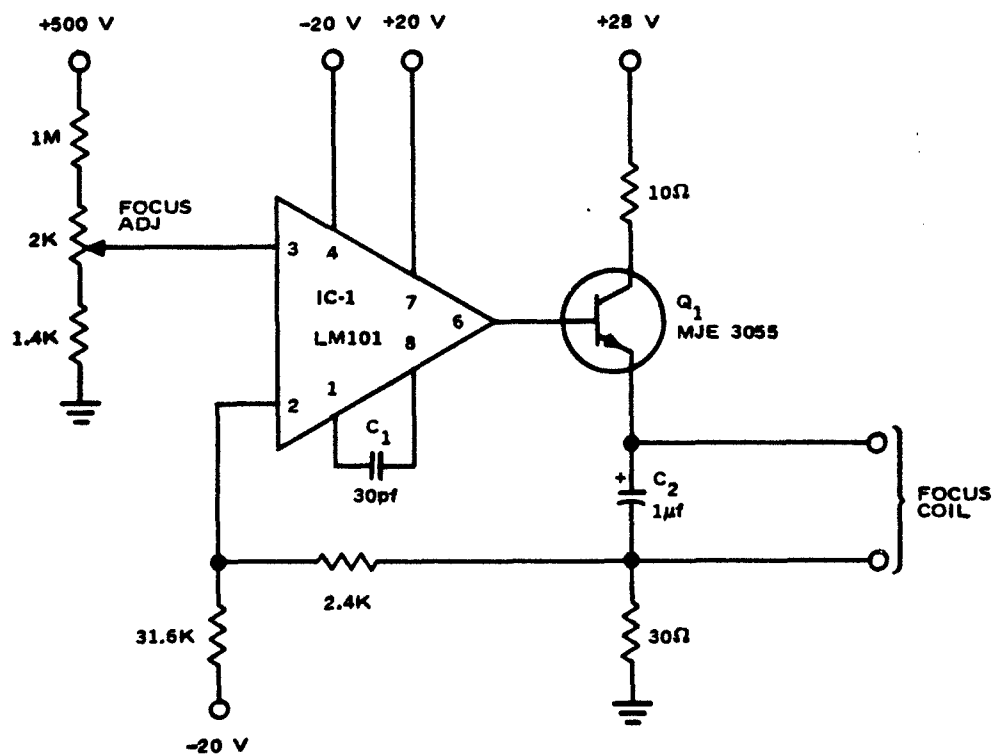
BLANKING

(U) FIG. 8. Vidicon Blanking and Sweep-Failure Protection.



(U) FIG. 9. High-Voltage Electrode Supply.

be highly stable, however, and low-temperature-coefficient, metal-film resistors are used throughout.



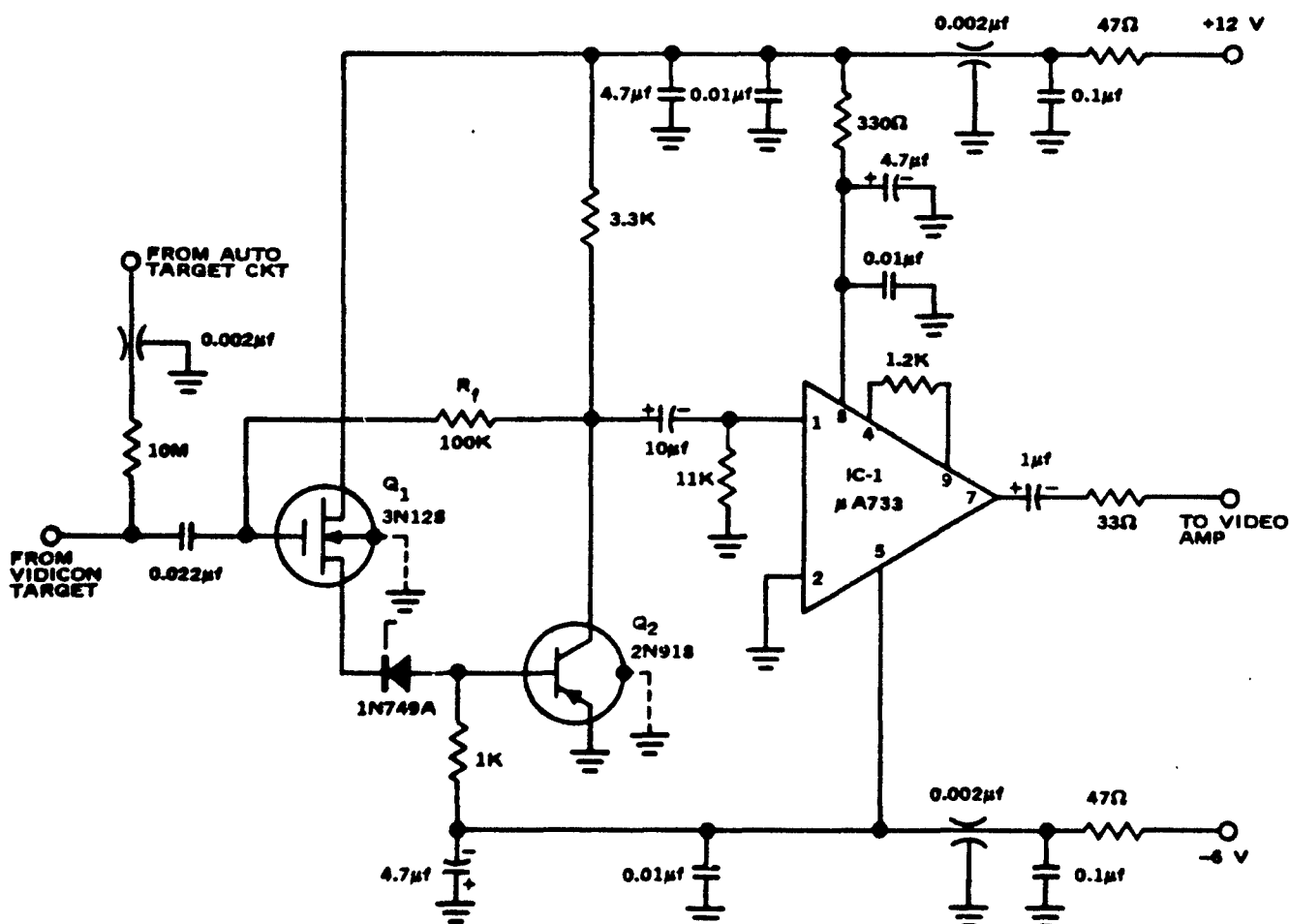
(U) FIG. 10. Focus Regulator Circuit.

VIDEO AMPLIFIER

(U) The video amplifier is one of the most complicated parts of the camera system. In addition to providing wide-band gain, it must incorporate keyed-clamping, black-clipping, sync-pulse addition, auxiliary outputs for trackers and automatic target control, and an output stage for low-impedance line driving.

(U) The starting point of the video amplifier chain is the preamplifier. The necessity for low capacitance at the input requires that it be mounted at the vidicon target terminal. Space limitations require the rest of the video amplifier to be mounted elsewhere, resulting in two sections.

(U) The preamplifier is a design used extensively in experimental Walleye guidance units and can be considered well-developed. The electrical diagram is shown in Fig. 11. The MOS transistor Q_1 is a 3N128. It has proved to be low in flicker noise and has high RFI rejection. The feedback amplifier, composed of Q_1 and Q_2 , has approximately a 10-megahertz bandwidth. The output amplifier,



(U) FIG. 11. Video Preamplifier Electrical Diagram.

IC-1, raises the level to 0.15 volt, peak-to-peak, and drives about 200 picofarads of line capacitance to the rest of the video amplifier.

(U) Considerable care is required in the layout of this amplifier since the bandwidth is almost totally a function of parasitic circuit capacitance, particularly that shunting the feedback resistor, R_f . The input-shunt capacitance and the 2N918 output-load capacitance, with the feedback network, cause a two-pole response. The damping can be controlled by the shunt capacitance of R_f and its distributed capacitance to ground.

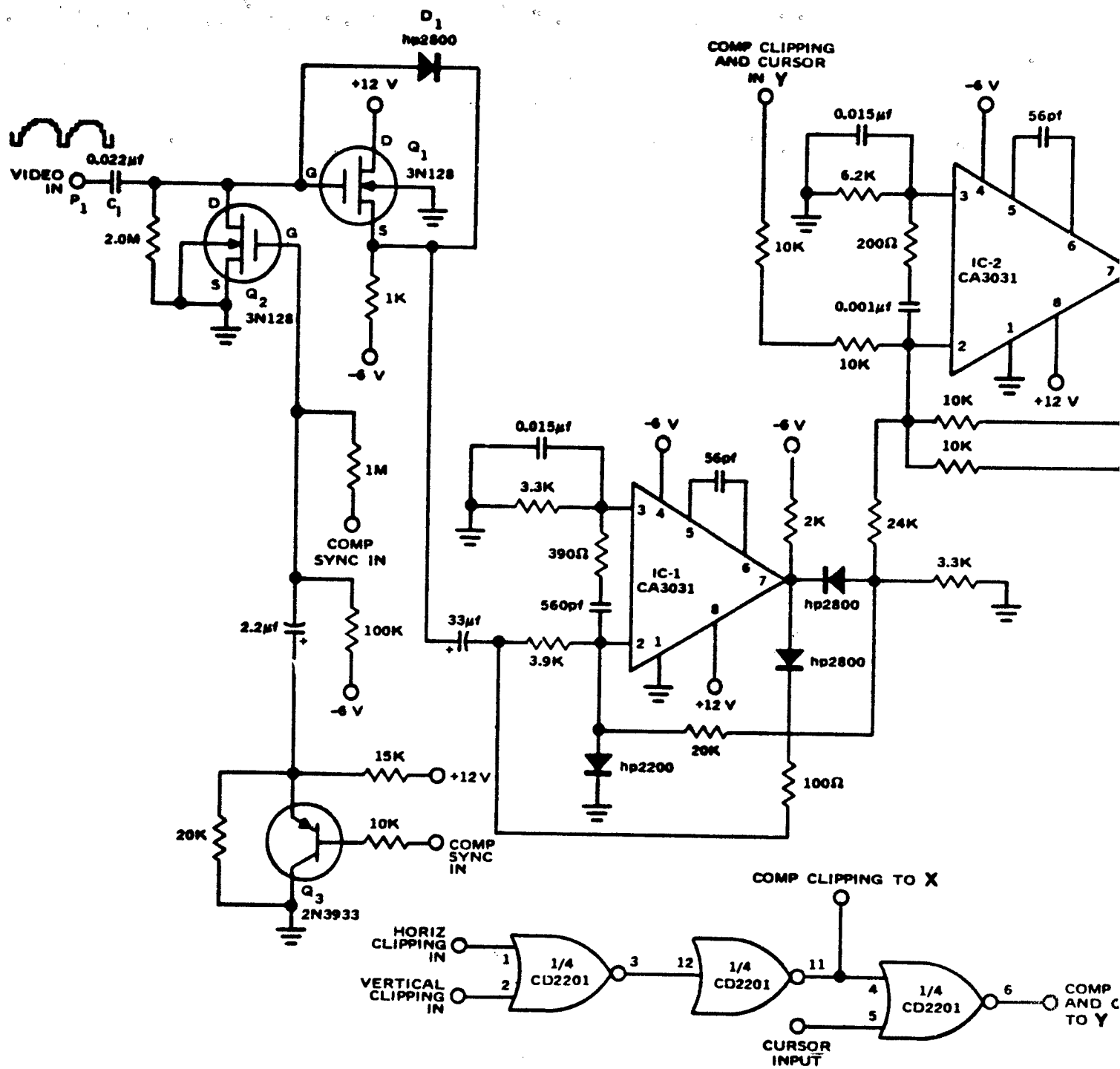
(U) The amplifier must be completely shielded and all power supply leads must enter by feed-through bypass capacitors. The output end must be as remote as possible from the input terminal and the mesh electrode of the vidicon adequately bypassed to the amplifier ground terminal.

(U) The preamplifier output is connected to the video amplifier chain (Fig. 12) via coaxial cable. The cable is not terminated for lengths of 5 feet or less. The cable feeds directly into the keyed-clamp circuit, Q_1 and Q_2 . Transistor Q_2 is a bidirectional switch, driven by the composite sync and charges C_1 to the video black level during horizontal and vertical retrace. Transistor Q_1 is a source follower after the clamp. The clamped output is fed to a DC restorer composed of IC-1 and its associated components. The output is white-negative and has an accurately restored black level.

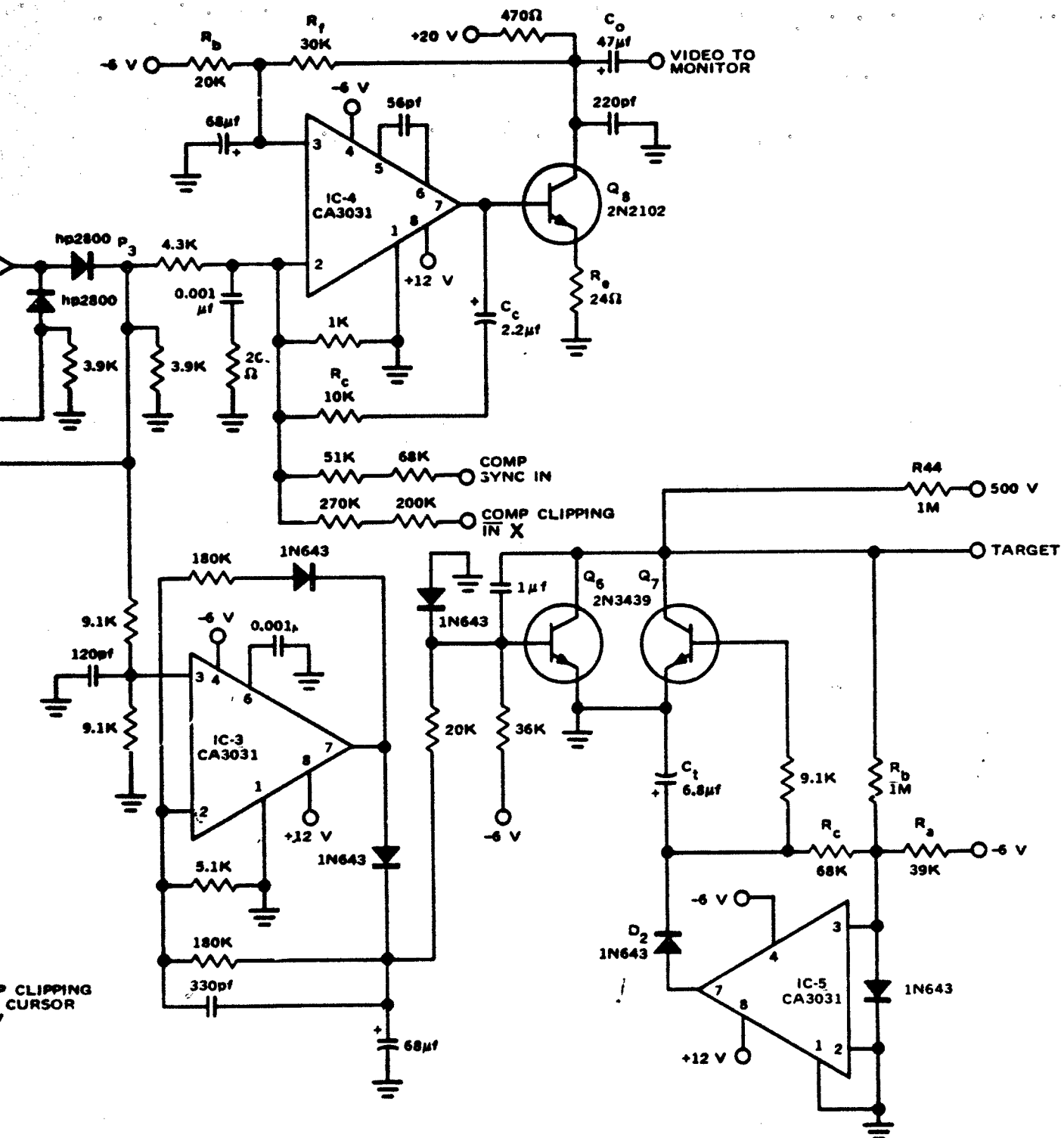
(U) The next stage is the black clipper, composed of IC-2 and associated components. This inverting amplifier is capable of positive output only, so that any negative or blacker-than-black signals are clipped at zero volt. This stage is used to remove the large white signals occurring at the raster edges (an unavoidable effect) and any other signals within the clipping interval. The clipping is accomplished by summing the large, positive clipping signal into the amplifier input, which drives the amplifier toward a negative output. Since the output can only go to zero, any negative output is clipped at zero volt. This assures a zero signal during the interval normally reserved for blanking. Strobe, cursor, or crosshair markers can be added to this stage as black lines. The clipping at zero assures that the markers do not extend into the sync level. A photograph of the output of this stage (point P₃, Fig. 12) is shown in Fig. 13 in which the black clipping interval can be seen. Note the absence of any blacker-than-black levels.

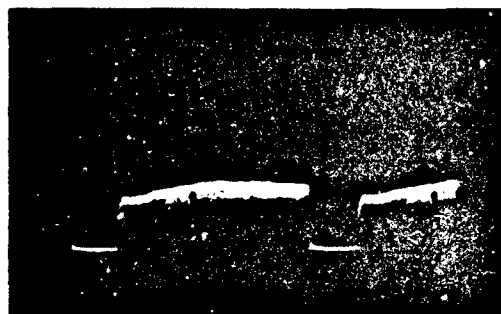
(U) The output stage contains IC-4 and Q_8 . The main functions of this stage are to add sync pulses and the pedestal level to the video and to drive a 75- or 91-ohm line at a 3-volt, peak-to-peak, level.

(U) Component IC-4 operates as an inverting voltage amplifier driving Q_8 . The gain of Q_8 is the ratio of (R_{Load}/R_e), and is again inverting. The operating point of the output stage is set by the DC feedback loop from the Q_8 collector through R_f to the noninverting input

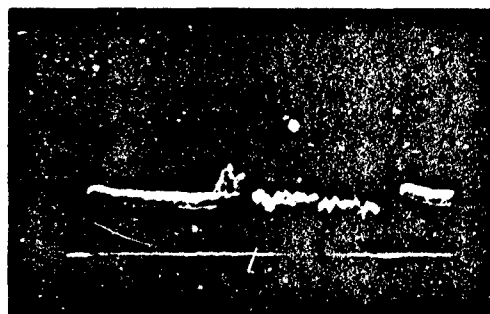


(U) FIG. 12. Video





(a)



(b)

(U) FIG. 13. Voltage Waveforms at P_3 , Fig. 12. (a) Horizontal waveform showing clipping interval. Scope set at $10 \mu\text{sec/cm}$; 0.1 V/cm . (b) Vertical waveform showing clipping interval. Scope set at 2.5 ms/cm ; 0.1 V/cm .

of IC-4. A bias input through R_b then sets the Q_g collector voltage. The output impedance of Q_g is approximately the collector load resistance of 470 ohms, hence, the line is driven from a relatively high impedance source. This advantageously reduces the effect of ground-return voltages that might exist between the amplifier output and the display device. These voltages will be attenuated by the ratio $(R_{\text{line}}/R_{\text{line}} + 470 \text{ ohms})$, or, in this case, by a factor of 6. Another advantage of this stage is that it cannot be damaged by a short circuit on the output. Also, if the stage is terminated by two or more display devices in parallel, the output level will reduce proportionately, but will not clip or become non-linear. It is stable with any type of termination and has proved to be an excellent choice for this camera. The voltage output into a 75-ohm load is shown in Fig. 14. The pedestal level and sync pulse have been added. The low-frequency response droop, due to the small output coupling capacitor C_o (Fig. 12), is compensated by the feedback network $R_c C_c$.



(a)



(b)

(U) FIG. 14. Voltage Output Waveforms Into a 75-Ohm Load. (a) Horizontal waveform. Scope set at $10 \mu\text{sec/cm}$; 1 V/cm . (b) Vertical waveform. Scope set at 2.5 ms/cm ; 1 V/cm .

(U) The automatic target control is not a part of the video amplifier, however, it is constructed on the same printed-circuit board and derives its input from the video amplifier. The circuit comprises IC-3, IC-5, Q₆, and Q₇. A peak detector (IC-3) measures the peak video level. The true peak is smeared out by a bandwidth restriction in IC-3 to prevent small, white objects from causing a large peak voltage. A current proportional to the peak voltage is summed with a reference current at the base of Q₆. If the signal current is greater than the reference current, the Q₆ collector voltage changes at a rate proportional to the difference. This lowers the vidicon target voltage until the signal and reference currents are equal. Thus, the circuit is a closed-loop feedback regulator.

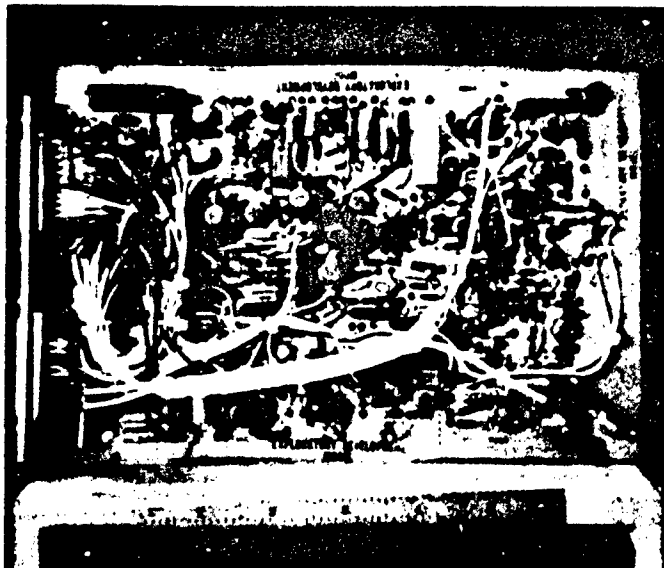
(U) An anomalous condition can occur in this system. If the vidicon target voltage becomes excessively high, an inversion of video polarity results and the signal level falls to a low value, causing a lock-up of the regulator; that is, the regulator will go to full output in an attempt to raise the video level, which it can no longer do. This situation occurs when the system is first energized and the vidicon filament is heating.

(U) A partial solution to the problem would be to limit the maximum voltage of the vidicon target, so that it would not saturate. Unfortunately, the saturation voltage varies widely with a variety of vidicons operating over a large temperature range. In this instance, the method used to avoid lock-up is to detect when the target voltage has risen to a value that will saturate any tube and then rapidly reset it to zero. The regulator will then slowly raise the target voltage until the video level is correct and hold it at that point. The reset circuit uses IC-5 and Q₇. The output of IC-5 is normally low, since it is biased by R_a from the -6 volts to the noninverting input. An input from the target voltage through R_b will, at a precise value, cause the net input to go positive. The output then goes high, charges C_t through D₁ and causes lock-up at IC-5 by positive feedback resistor R_c. The voltage on C_t causes Q₇ to conduct and the target voltage is rapidly reduced to zero. The diode D₂ prevents the amplifier from discharging C_t so that Q₇ may have time to discharge the target circuit. When the target voltage has dropped, IC-5 output is negative and the target regulator can take over control. With no video present, the recycle rate is about 1 hertz.

RESULTS

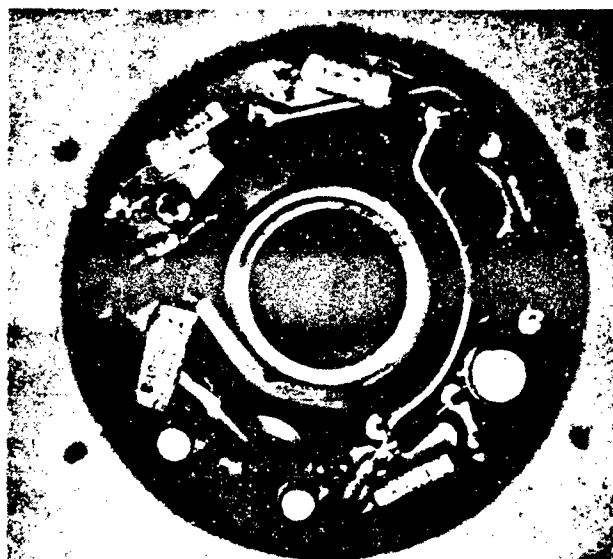
(U) All of the circuitry described (except the preamplifier) is constructed on a single printed-circuit board. This system has been

successfully reproduced over fifteen times at NWC and the Naval Avionics Facility, Indianapolis, one of whose modules is shown in Fig. 15.



(U) FIG. 15. Circuitry Layout on a Single Printed-Circuit Board.

(U) A typical preamplifier layout is shown in Fig. 16. This fits around the target flange of the vidicon and inside a shielded enclosure that holds the tube and optics.



(U) FIG. 16. Typical Preamplifier Layout.

(U) Environmental testing showed that the circuitry would operate from -55 to +125°C, which is beyond the capability of the vidicon. Three of the new cameras accumulated over 100 hours of flight time in an A-4 aircraft. (Flight conditions covered the maximum performance of the aircraft relative to altitude, speed, and vibration.) Two electrical failures occurred during the flights. One failure was due to the MOS transistor Q₁ in the video amplifier keyed-clamp. The addition of diode D₁ eliminated the cause of the failure by preventing the gate-to-source voltage from going positive.

(U) The second failure, that of the horizontal deflection, occurred because the output transistors were not provided with adequate heat sinks. As a corrective measure, finned radiators were placed on the transistors to reduce temperature. The latest device incorporating these design changes recorded 25 hours of flight time, during which no changes or adjustments were necessary.

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13. ABSTRACT

(U) A description of an improved television camera for the Walleye missile with emphasis on the electronic circuitry.

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ABSTRACT CARD

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A description of an improved television camera for the Walleye missile with emphasis on the electronic circuitry.

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An Improved Walleye Television Camera (U), by William Woodworth. China Lake, Calif., NWC, May 1970. 18 pp. (NWC TP 4944, publication CONFIDENTIAL.)

A description of an improved television camera for the Walleye missile with emphasis on the electronic circuitry.

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